CPRE 4910 Weekly Report 04

10/14/2025 - 10/20/2025

Group number: SDMay26-24

Project title: Digital ASIC Fabrication

Client &/Advisor: Dr. Henry Duwe

Team Members/Role:

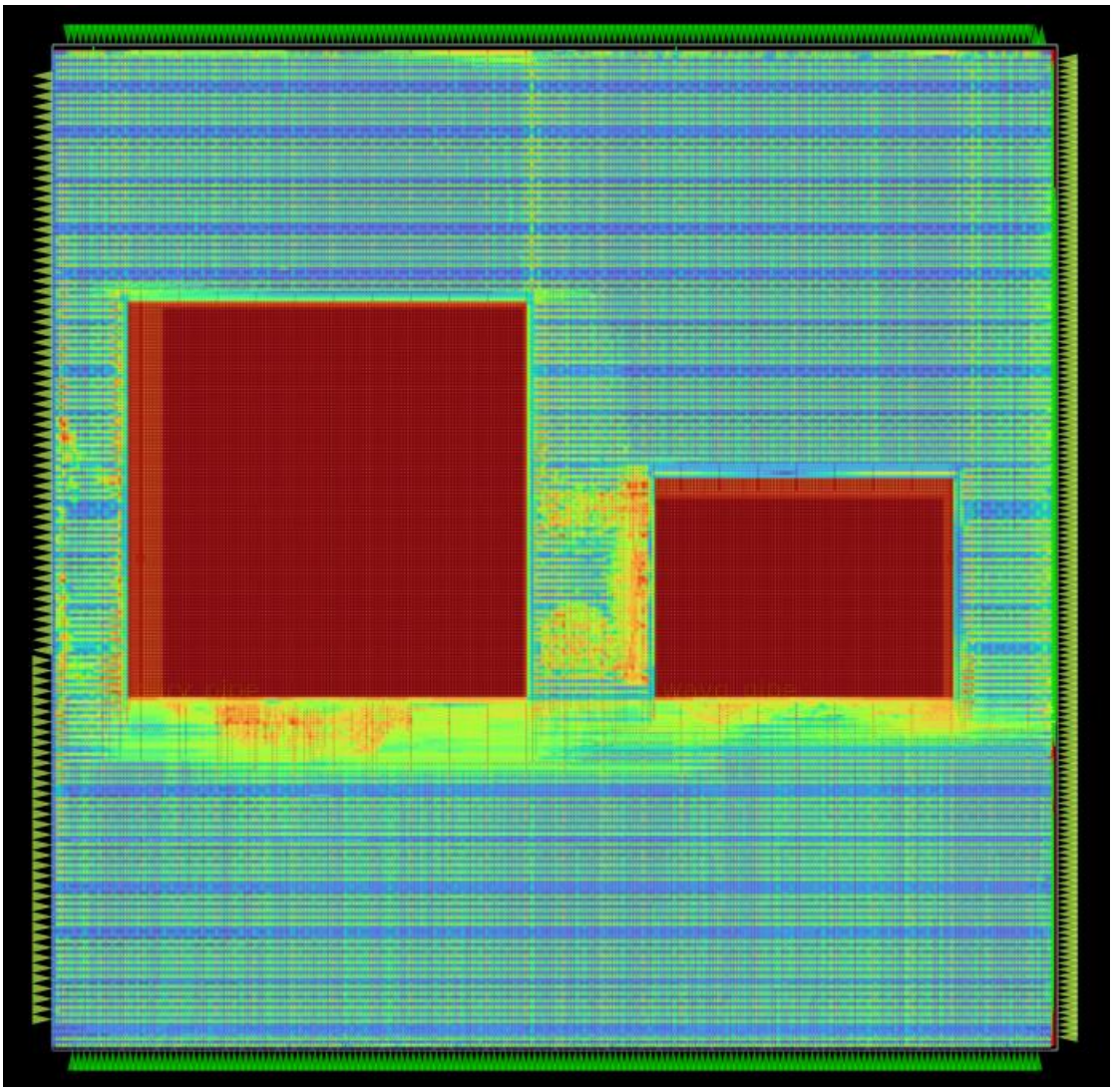
Colin McGann	***-Project Lead***
Samuel Forde	***-PCB & Layout Lead***
Michael Drobot	***-Firmware Lead***
Jack Tonn	***-Testbench and Validation Lead***
Dawud Benedict	***-Toolflow Lead***
Emil Kosic	***-Repository and Coding Standards Lead***
Joshua Arceo	***-Client/Advisor Communications Lead***

- **Weekly Summary**

This week we integrated the Sky130 PDK into Cadence to improve our synthesis results, designed the VGA output Verilog module, researched vertex and fragment shader programs, and continued planning out our custom cores and ISA.

- **Past Week Accomplishments**

- Colin McGann: Continued work on the rasterizer by updating it to work with our new stream system. Also synthesized the rasterizer and sub-components.



- Jack Tonn: Wrote SVUnit guide and showed others how to use it. Also built test infrastructure to place all tests in the same directory to allow for easy regression testing, with the idea of allowing CICD through the output of the tests XML file, given after running a group of tests.
- Dawud Benedict: Got Sky130 PDK to work with Genus and Innovus. Synthesis outputs no errors, and the schematic view appears correct. PnR is still in work, but cells are being placed without error. It still needs to be tested in the layout process.
- Michael Drobot: Finished design of VGA module, got it to pass testbenches and RTL. Still working on getting it to pass hardening. Also worked with Colin and Emil to get the cores and ISA planned out.

- Sam Forde: Gave presentation on vertex shading, how it works, and considerations. Also worked on writing mac unit, and other variations on matrix multipliers.
- Josh Arceo: Completed chipforge tutorials, began working on fragment shader c code
- Emil Kosic: Familiarization of vertex shading architecture, improving vertex shader implementation code to take in a custom image and output values needed for working rasterizer to test against.

- **Pending Issues**
  - Confirm Cadence tools will work for tapeout.
  - Fix VGA module hardening issues.
  - The VGA module is really big, look into OpenRAM to make it smaller.

- **Individual contributions**

NAME	Individual Contributions	Hours this week	HOURS cumulative
Colin McGann	Rasterizer synthesis & testing	10	65
Jack Tonn	Wrote SVUnit guide and infrastructure	4	30
Dawud Benedict	Get Innovus and Genus working with Sky130	7	27
Michael Drobot	Finish VGA module RTL, start hardening	18	40
Sam Forde	Vertex shading presentation, writing verilog units	8	26
Josh Arceo	Completed chipforge tutorials, fragment shader c code	5	20
Emil Kosic	Refactored vertex shading code to closer real implementation	4	21

- **Plans for the upcoming week**
  - Colin McGann: Finishing the rasterizer and starting work on a FPGA demo
  - Jack Tonn: Teach verification flow, start writing testing section of design document.
  - Dawud Benedict: Send PnR output to Colin to test. Continue working on HDL.
  - Michael Drobot: Get VGA to harden, look into OpenRAM to replace the VGA line cache and for ChipForge use.

- Sam Forde: Learn verification flow, look into pipelining multiply and accumulate unit(mac), and aim to have performance comparisons between units if possible.
- Josh Arceo: Finish fragment shader C code, begin converting to our custom assembly
- Emil Kosic: Complete full vertex shader code, create custom ISA instructions for vertex shading and begin building core in Verilog.